Amendments To The Specification

Please replace the paragraph in the specification on page 27, line 28 to page 28, line 4 with the following amended paragraph:

As shown in FIG. 4C, openings 37 are formed in predetermined positions in the first insulation layer **[[25]] --26--** corresponding to the rewiring layers 23. While each opening 37 is formed on an end of the corresponding rewiring layer 23 opposite to the end connected to the post electrode 22A, the opening 37 may be formed in an arbitrary position. It is to be noted that the openings 37 can be formed by etching, laser processing, or the like.

Please replace the paragraph in the specification on page 28, line 21 to page 29, line 5 with the following amended paragraph:

In the post electrode forming process performed after the integrating process, the ~~substrate~~ **post electrodes** 22A are formed inside the through holes 31A. Since these post electrodes 22A are formed directly on the barrier metal portions 14 (electrodes 13) of the semiconductor chip 11, impedance between the semiconductor chip 11 and the interposer 20A can be reduced, thereby improving electrical properties. Moreover, since the post electrodes 22A are formed using the through holes 31A (on whose inner surface the first insulation layer 25 is actually formed) formed in the interposer base 21A as molds, the post electrodes 22A can be easily formed.

Please replace the paragraph in the specification on page 33, lines 5-14 with the following amended paragraph:

Barrier metal portions 14 are exposed at the bottom of the through holes. Then, copper plating is performed to form the post electrodes **[[22A]] --22B--** inside the through holes formed in the dry film. The post electrodes **[[22A]] --22B--** are formed directly on the barrier metal portions 14 (electrodes 13). The dry film is then removed, so that the semiconductor chip 11 on which the post electrodes 22B are formed as shown in FIG. 8A is manufactured.

Please replace the paragraph in the specification on page 33, lines 15-29 with

the following amended paragraph:

After the post electrode forming process is completed, the integrating process is performed. In the integrating process, the semiconductor chip 11 and the interposer base **[[21B]] --21A--** are placed in a vacuum unit, and smooth surfaces (mirror surfaces) of the semiconductor chip 11 and the interposer base 21A are brought into contact with and pressed against each other in a predetermined vacuum environment. The smooth surfaces are thus put in tight contact with each other and integrated with each other without using adhesive or the like. As a result, as shown in FIG. 8B, the semiconductor chip 11 and the interposer base **[[21B]] --21A--** are securely joined together.

Please replace the paragraph in the specification on page 33, line 30 to page 34, line 6 with the following amended paragraph:

When the semiconductor chip 11 and the interposer base **[[21B]] --21A--** are integrated with each other, the post electrodes 22B are inserted in the through holes 31A formed in the interposer base 21A. The diameter of the post electrodes 22B is smaller than the diameter of the through holes 31A, and therefore gaps are formed between the outer circumferential surfaces of the post electrodes 22B and the inner circumferential surfaces of the through holes 31A.

Please replace the paragraph in the specification on page 36, lines 25-31 with the following amended paragraph:

As in the case of the semiconductor device 10D of the **[[third]] --fourth--** embodiment, the semiconductor device 10E of this embodiment is configured such that plural post electrodes 22B are disposed in one through hole 31B. The post electrodes 22B are formed directly on barrier metal portions 14 (electrodes 13).

Please replace the paragraph in the specification on page 39, lines 2-12 with the following amended paragraph:

The following describes sixth - eighth embodiments of the present invention. FIG. 13 shows a semiconductor device 10F of the sixth embodiment. FIG. 14 shows a semiconductor device 10G of the seventh embodiment. FIG. 15 shows a semiconductor device 10H of the eighth embodiment. The semiconductor devices **[[10G]] --10F--** – 10H of these embodiments are configured to be reduced in thickness compared to the semiconductor devices

10A – 10E of the above-described first – fifth embodiments.

Please replace the paragraph in the specification on page 40, line 31 to page 41, line 4with the following amended paragraph:

The semiconductor devices 10I – 10L shown in FIGS. 16 – 20 are characterized in that plural semiconductor chips 11 are disposed on corresponding interposers 20I – 21H. In FIG. 16 and the figures that follow, elements identical to those in FIGS. **[[1A]] –1--** – 4D bear the same reference numbers and are not further described.

Please replace the paragraph in the specification on page 43, lines 16-32 with the following amended paragraph:

As in the case of the semiconductor device 10J of the ~~eleventh~~ **tenth** embodiment shown in FIG. 18, the semiconductor device 10K of this embodiment is configured such that the openings 43 are formed in positions on the top plate section 42 of the interposer base 21G facing back faces 11a of the semiconductor chips 11, and therefore heat releasing efficiency of the semiconductor chips 11 is increased. However, although the heat releasing efficiency is increased by forming the openings 43, the size of the joining area between the top plate section 42 and the semiconductor chips 11 is reduced. Accordingly, compared to the semiconductor device 10J shown in FIG. 18, the semiconductor chips 11 are less firmly joined to the interposer base 21G.

Please replace the paragraph in the specification on page 44, lines 13-26 with the following amended paragraph:

The semiconductor device 10L of the twelfth embodiment shown in FIG. 20 is configured such that plural cavities **[[40B]] --40C--** are formed in the interposer base 21H from the upper surface thereof, and a through hole 31D is formed in a bottom plate section 45 of each cavity **[[40B]] --40C--**. An insulation film 15 of the semiconductor chip 11 is joined to the bottom plate section 45 around the through hole 31D by small base surface joining, and thus secured to the interposer base 21H. Post electrodes 22A are configured to extend through the corresponding through holes 31D to the lower surface side of the interposer base 21H.

Please replace the paragraph in the specification on page 45, lines 13-17 with

the following amended paragraph:

The semiconductor devices 10M and 10N shown in FIGS. 21 - 23 are characterized in that joint reinforcing members 27 are provided in order to join semiconductor chips 11 to interposers ~~20G and 20H~~ **20M and 20N** more securely.

Please replace the paragraph in the specification on page 45, line 31 to page 46, line 15with the following amended paragraph:

The semiconductor device **[[10M]] --10N--** of the fourteenth embodiment shown in FIG. 23 corresponds to the semiconductor device 10J of the tenth embodiment shown in FIG. 18, but the joint reinforcing members 27 are provided. The joint reinforcing members 27 are disposed between the upper surface of a top plate section 42 in a cavity 40C and back faces 11a of the semiconductor chips 11 and between the lower surface of the top plate section 42 and the outer circumferential surfaces of the semiconductor chips 11. Therefore, in the semiconductor devices 10M and 10N of the thirteenth and fourteenth embodiments, mechanical strength of the semiconductor chips 11 against interposer bases 21H and 21G can be increased while maintaining high heat releasing efficiency of the semiconductor chips 11.

Please replace the paragraph in the specification on page 48, lines 11-18 with the following amended paragraph:

The semiconductor devices 10Q and 10R shown in FIGS. 26 and 27 are characterized in that the sealing resins 46B are formed by molding. Forming the sealing resins 46B by molding can increase the degree of freedom of the shape of the sealing resins **[[46A]] --46B--** compared to the method of forming the sealing resin 46A shown in FIGS. 24 and 25 by screen printing.

Please replace the paragraph in the specification on page 49, lines 15-23 with the following amended paragraph:

In the electronic devices 10A – 10R of the above-described embodiments, the semiconductor chips 11 are used as electronic elements to be mounted on the interposer bases 21A – **[[20I]] --21I--**. On the other hand, in the eighteenth – twentieth embodiments, chip parts 50A – 50C as passive elements are used as electronic elements. Examples of the chip parts 50A – 50C include chip capacitors, chip resistors, etc.

Please replace the paragraph in the specification on page 51, line 26 to page 52, line 2 with the following amended paragraph:

In the electronic devices (semiconductor devices) 10A – 10R of the above-described embodiments, the semiconductor chips 11 are used as electronic elements to be mounted on the interposer 20A – 20R. In the electronic devices 10S – **[[10V]] --10U--** of the eighteenth embodiment – twentieth embodiments, the chip parts 50A – 50C as passive elements are used as electronic elements to be mounted on the interposer 20S – 20U.